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Fax No.	:	571-273-8300
Attention	:	**EXAMINER : NADAV, ORI**
Group Unit	:	2811
From	:	Jiawei Huang, Reg. No. 43,330
MESSAGE	:	Enclosed herewith is a Reply Brief in 10 pages.

Sir:

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on **April 8, 2008** at the above indicated fax number.

Sign by: _____
Jiawei Huang

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner : NADAV, ORI

Group Art Unit : 2811

In re PATENT APPLICATION of
Applicant : Chun-Hsiang Lai et al.

Serial No. : 09/801,350

Filed : March 07, 2001

For : ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT COUPLED ON I/O PAD

Attorney Docket: JCLA6643-R3

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APPELLANT'S REPLY BRIEF

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to Examiner's Answer dated February 8, 2008 under 37 C.F.R.41.41.

A careful analysis of the Examiner's answer ("the Answer") brings out many points to reply.

Appellant respectfully traverses the Examiner's assertions as discussed below.

1. Claim 1 Is Not Anticipated By Lin

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). For a prior art reference to anticipate a claim, the reference must disclose each and every element of the claim with sufficient clarity to prove its existence in the prior art. Motorola, Inc v. Interdigital Tech. Corp., 121 F. 3d 1461, 43 USPQ 2d 1746, 1749 (Fed. Cir. 1991).

The Answer stated, on pages 11-12, that the circuit/drawing is identical to the circuit depicted in Figure 6A of Lin (with exception of Appellant's diode 108 which is connected between the I/O pad and voltage source), wherein the first connection terminal line and the fourth connection terminal line are also connected to one common horizontal line which branches out to the I/O pad (PAD) and the voltage source Vh. The Answer also stated that clearly Lin does not teach that the I/O pad, the voltage source Vh and the voltage bus Vdd are all the same element. The fact that the first connection terminal line and the fourth connection terminal line of Lin (and of Appellant) are connected to one common horizontal line which branches out to the I/O pad and the voltage source, does not mean that the I/O pad and the voltage source are the same element.

Appellant respectfully disagrees with the Examiner's interpretation that "the first connection terminal line and the fourth connection terminal line of Lin, which are connected to one common horizontal line which branches out into the I/O pad and the voltage source, would also mean that the common line of Lin to be two separate elements, namely the I/O pad and the voltage source", and respectfully submits that when two devices A and B are shown in the drawing(s) to be connected to a common horizontal line, one skilled in the art would normally interpret that both A and B are connected to the SAME ELEMENT, namely "the common horizontal line" regardless whether or not the common horizontal line branches into two or more branches.

Thus, because Lin substantially discloses that both the first connection terminal line of the SCR circuit and the fourth connection terminal line of the transient oscillator circuit 61 are respectively connected to the VDD bus or the I/O pad (please see FIG. 6A and 9), and therefore, it is clearly evident that Lin substantially fails to teach or disclose

that the first connection terminal line of the SCR circuit is connected to the I/O pad and the fourth connection terminal line of the transient circuit is connected to the voltage source.

Appellant respectfully submits that it is impermissible, however simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements to fill the gaps, and any such reconstruction to depreciate the claimed invention would be construed as hindsight reconstruction.

Therefore, Lin cannot anticipate the proposed independent claim 1 because Lin fails to teach, disclose or show each and every elements of the proposed independent claim 1. More specifically, the Appellant respectfully submits that Lin fails to teach or disclose that the first connection terminal and the second connection terminal of the SCR circuit are respectively connected to the I/O pad and a ground voltage, and the fourth connection terminal, the fifth connection terminal, and the sixth connection terminal of the anti-latch-up circuit are respectively coupled to the voltage source, the ground voltage, and the third connection terminal of the SCR circuit as recited by the proposed independent claim 1.

The advantage of connecting the (fourth connection terminal of the) anti-latch-up circuit to the voltage source and connecting the (first connection terminal of the) SCR circuit to the I/O pad is that only one anti-latch-up circuit is required for several I/O pads, and therefore, the space occupation on the integrated circuit can be effectively reduced.

Thus, the structure of the ESD protection device of Lin is substantially different compared to the structure of the ESD protection device of the present invention.

Accordingly, Lin cannot possibly anticipate the proposed independent claim 1, and therefore the proposed independent claim 1 patentably defines over Lin, and should be allowed.

2. Claim 1 Is Not Rendered Obvious By Quiley

The Answer stated, on pages 12-13, that as discussed above, both Appellant and Lin teach a first connection terminal line and a fourth terminal line being connected to a

common horizontal line which branches out to an I/O pad and a voltage source. Quigley also teaches in Figure 1 a first connection terminal line and a fourth connection terminal line being connected to one common horizontal line, which branches out to an I/O pad and a voltage source, for the following reasons:

It is clear from Figure 1 that Quigley teaches a first connection terminal of the SCR circuit 22 being connected to an I/O pad. Quigley further teaches a fourth connection terminal of an anti-latch-up circuit RC 17, 18 being coupled to the common horizontal line. The common horizontal line is coupled to a voltage source for the following reasons: a device would not function without a voltage source and a ground connection. Therefore, although Figure 1 of Quigley does not depict both the voltage source and the ground connection, these connections must be inherent in Quigley's device. That is, a voltage drop must be present between the "Vss" node and the horizontal line connected to the pad. Furthermore, Quigley teaches that the RC circuit 17, 18 is a voltage divider. That is, a voltage must exist across the RC circuit, i.e. between the "Vss" node and the horizontal line connected to the pad. This voltage can also be considered as a voltage source to the device. Thus, since a voltage to operate the device must be present at the horizontal line, then Quigley teaches a fourth connection terminal of an anti-latch-up circuit RC 17, 18 being coupled to a voltage source, as claimed.

Appellant respectfully disagrees with the Examiner's interpretation that "a voltage drop must be present between the "Vss" node and the horizontal line connected to the pad" and that "a voltage must exist across the RC circuit, i.e. between the "Vss" node and the horizontal line connected to the pad, and this voltage can also be considered as a voltage source to the device", and thus, since a voltage to operate the device must be present at the horizontal line, then Quigley teaches a fourth connection terminal of an anti-latch-up circuit RC 17, 18 being coupled to a voltage source, as claimed".

First, Appellant would like to point out that the voltage divider comprising the capacitor 17 and the resistor 18 is connected between the Vss node and the horizontal line. In the Quigley's ESD protection device 11, during an ESD event, because the voltage exceeds the threshold voltage, the ESD couples through the capacitor 17 and generates an voltage across the resistor 18, which in turn triggers the SCR 22 in order to

short the pad to the Vss to protect the internal circuitry. In other words, the voltage across the resistor is the voltage that flows across the (voltage divider) device itself, and this voltage is supplied from the I/O pad supplies the voltage to the voltage divider (17, 18) when the ESD attacks the I/O pad. In other words, Quigley substantially shows that both the voltage divider (17, 18) and the SCR 22 are connected to the I/O pad. And, the fact that the claim 1 recites that "the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the anti-latch-up circuit is connected to a voltage source" would imply that the voltage source is other than the I/O pad, and that the I/O pad and the voltage source are two separate elements (this is well supported in FIG. 4 of the present invention). Thus, Appellant respectfully submits that Quigley substantially fails to teach or disclose the first connection terminal line SCR 22 is connected to the I/O pad; and the forth connection terminal line of the voltage divider (17, 18) are respectively connected the I/O pad and the voltage source, as required by claim 1, instead Quigley substantially shows that both the voltage divider (17, 18) and the SCR 22 are connected to the same I/O pad.

In the claimed invention, as clearly recited in claim 1, and also as clearly shown in Figure 4, the first connection terminal (112) of the SCR circuit (104) is connected to "a I/O pad" (100); and the fourth connection terminal (126) of the anti-latch-up circuit (110) is connected to "a voltage source" (Vcc). The language "the first connection terminal (112, of the SCR circuit) is connected to a I/O pad" and "fourth connection terminal (126, of the anti-latch-up circuit) is coupled to a voltage source (Vcc)" clearly indicate that the I/O pad and the voltage source are TWO separate elements, and that the first connection terminal of the SCR circuit and the fourth connection terminal of the anti-latch-up circuit are respectively connected to two different elements, namely, the I/O pad and the voltage source, which is also fully supported by Figure 4.

Thus, the structure of the ESD protection device of Quigley is substantially different compared to the structure of the ESD protection device of the present invention.

Accordingly, as discussed above, both Lin and Quigley, neither alone nor in combination, can possibly disclose, teach or suggest every features of the proposed independent claim 1 in this regard, and therefore the proposed independent claim 1 patentably defines over Lin and Quigley and should be allowed.

3. Claim 15 Is Not Rendered Obvious By Quigley and Lin

The Answer stated, on pages 13-14, that although Quigley sets the threshold voltage for triggering the SCR circuit and prolongs the delay time of the SCR circuit to prevent normal signals from triggering the SCR circuit, Lin provides an advantageous reason to further modify and fine tuning the parameters of the capacitor and the resistor of the RC circuit so that the SCR is easier to be triggered during an ESD event, and that the SCR does not trigger during the normal operation or powering up.

Furthermore, the Examiner stated that Lin explicitly teaches that using an RC relay time of the RC anti-latch-up circuit larger than the voltage rising phase of the ESD transient would more easily trigger the SCR during an ESD event (column 4, lines 26-32). Lin further teaches that using an RC relay time of the RC anti-latch-up circuit less (smaller) than the powering up transient, would prevent the SCR from being triggered during normal operation or powering up. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power and greater than a voltage rising time of an ESD pulse, as taught by Lin, in Quigley, as claimed.

Appellant disagrees, and respectfully submits that Claim 15 recites the limitation "a RC delay time of the anti-latch up circuit smaller than a voltage rising time of the IC power but greater than the voltage rising ESD pulse". According to the present invention, when there is an accidental over-voltage or voltage surge during the normal IC operation, because the RC Delay Time of the anti-latch up circuit is designed to be smaller than a voltage rising time of the IC power, therefore the rising voltage of the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power so that a voltage level of the node A has the same voltage (Vdd). Thus, a large amount of carriers, due to accidental over voltage, may be accordingly absorbed and the latch-up phenomenon is avoided. On the other hand, during the ESD event, since the RC delay time of the anti-latch-up circuit is greater than the voltage rising time of the ESD pulse, therefore the rising voltage of the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to

protect the internal circuit. Therefore the SCR circuit may be triggered at a lower holding voltage.

Instead, Quigley, at col. 4, lines 41-62, substantially teaches that because gate oxide breakdown occurs when a 10 volt DC voltage is applied across the gate oxide or a 20 volt transient voltage, and therefore ESD protection circuit 11 must enable SCR circuit 22 before the pad reaches 20 volts because an ESD event is a transient phenomenon corresponding to the higher voltage for gate oxide breakdown. More particularly, Quigley, at col. 4, lines 50-62, substantially teaches that the transistor 16 is enabled for turning on transistor 12 when a voltage at node 21 exceeds the threshold voltage of the transistor 16 and thereby generates a voltage at the node 21 to trigger the SCR circuit 22. Thus, Quigley substantially proposes setting a threshold voltage of, for example, 12 volts, as trigger voltage at the pad, and when the voltage at the pad exceeds 12 volts, the SCR circuit 22 is triggered. Quigley utilizes a voltage divider circuit, including a capacitor 17 and a resistor 18, designed for generating a control voltage to SCR circuit 22 due to a transient voltage applied to the pad when the voltage at the pad exceeds threshold voltage 12 volts.

Furthermore, Quigley, at col. 7, lines 1-4, substantially teaches sufficiently prolonging the delay time of the SCR circuit 22 to prevent normal signals of the integrated circuit from triggering the SCR circuit 22.

Therefore, it is clear that the mechanism of preventing triggering and triggering of the SCR circuit of the claimed invention is substantially different from that of Quigley, in that the claimed invention does not set any threshold voltage for triggering the SCR circuit or prolong the delay time of the SCR circuit to prevent normal signals of the IC from triggering the SCR circuit as expressly taught by Quigley, instead the claimed invention proposes designing the RC Delay Time of the anti-latch-up circuit to be smaller than the voltage rising of the IC power but greater than the rising voltage time of the ESD pulse so that the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power to prevent triggering the SCR circuit , and during the ESD event, the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit.

Accordingly, Appellant respectfully submits that Quigley substantially teaches away from the claimed invention, and therefore Quigley cannot possibly suggest one skilled in the art to modify Quigley's ESD device in a manner suggested by the Examiner because any such modification of Quigley's device would frustrate its intended purpose. As such, Quigley is complete and functional in itself, so there would be no reason to modify ESD circuit of Quigley, and certainly not to modify the voltage divider of Quigley in the manner suggested only by the Examiner.

Accordingly, Quigley and Lin cannot possibly motivate one skilled in the art to modify the ESD circuit of Quigley, in a manner suggested by the Examiner, to meet claim 15, and therefore claim 15 patentably defines over Quigley and Lin in this regard.

Furthermore, Appellant respectfully submits that because Lin, at col. 3, lines 48-53, substantially discloses that the transient oscillator circuit 61 is employed for generating fast clocks with increasing oscillation amplitude during the initial phase of an ESD transient, and also, the voltage transition of the fast clocks has a ramp rate that of the ESD transient voltage's ramp rate (50-1000 nanoseconds), and therefore, it clear that Lin substantially fails to teach, suggest or hint that the anti-latch-up circuit has a RC delay time that is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse, as required by the dependent claim 15, instead, Lin substantially teaches the voltage transition provided by the voltage transition circuit (51) has a ramp rate that of the ESD voltage's ramp rate.

Accordingly, Lin cannot possibly motivate one skilled in the art to modify the ESD circuit of Lin in a manner suggested by the Examiner to meet the proposed claim 15 in this regard, and therefore the proposed claim 15 should be allowed.

4. Claim 15 Is Not Rendered Obvious By Lin

The Answer stated, on page 15, that Lin's statement that "the voltage transition provided by the voltage transition circuit (51) has a ramp rate faster than the ESD voltage's ramp rate", does not mean that Lin teaches "RC delay time smaller than the ESD voltage ramp rate". In fact, Lin teaches in column 4, lines 26-32 that "the time constant of R1C1>50 ns, such that the SCR is easy to trigger during an ESD event. R1C1 is also preferably less than the powering up transient, for example, R1C1 < 1 micros, such that the SCR does not trigger during normal operation or powering up."

An artisan reading this statement would be motivated to use an RC relay time of the RC anti-latch-up circuit larger than the voltage rising phase of the transient so that the SCR is easy to trigger during an ESD event. An artisan would also be motivated to use an RC relay time of the anti-latch-up circuit less (smaller) than the powering up transient so that the SCR does not trigger during normal operation or powering up. Therefore, it would have been obvious to an artisan to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power and greater than a voltage rising time of an IC power and greater than a voltage rising time of an ESD pulse in Lin's device, as claimed.

Appellant respectfully submits that the typical voltage rising time of an IC device after being turned on is about a few milliseconds, i.e. more than 1000 microsecond or more than 1 millisecond, and the typical voltage rising time of an ESD pulse is in nanoseconds. As the Examiner has noted that Lin expressly teaches in column 4, lines 26-32 that the time constant of R1C1>50 ns, such that the SCR is easy to trigger during an ESD event, and the R1C1 is also preferably less than the powering up transient, for example, R1C1 < 1 microseconds, and therefore, it is clear that the time constant range of R1C1 of Lins' voltage transient circuit (51) is within 50-1000 ns. Therefore, the time constant range, 50-1000 ns, of R1C1, overlaps with that of the voltage rising time of an ESD pulse. Therefore, it is clear that Lin substantially fails to teach, suggest or hint that the voltage transient circuit has a RC delay time that is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse, as required by the dependent claim 15, instead, Lin substantially teaches the voltage transition provided by the voltage transition circuit (51) has a ramp rate of the ESD pulse. In other words, because Lin substantially teaches the voltage transition has RC delay time of the ESD pulse ramp rate, therefore, it is clearly evident that Lin substantially teaches away from the claimed invention in this regard.

CONCLUSION

As noted, none of the cited art, either alone or in combination, can be said to anticipate or render obvious the appealed claims. The references disclosing ESD protection circuit (Quigley, Lin, and Ker) fail to disclose, show, or suggest the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient circuit is connected to the voltage source (as recited in claim 1). Also, these references fail to disclose, show, or suggest ", and a RC delay

time of the anti-latch up circuit smaller than a voltage rising time of the IC power but greater than the voltage rising ESD pulse (as recited in claim 15)". The addition of Ker showing the first diode 70 and the second diode 60 is prior art, but does not cure the deficiencies of Lin and Quigley with respect to the connections of the transient circuit and the voltage divider respectively with respect to the I/O pad as discussed above.

Accordingly, Applicant believes that the rejections under 35 U.S.C. 102 and 103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

A decision directing the Examiner to issue a Notice of Allowance is respectfully requested.

Respectfully submitted,
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Date: 4-8-2008

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